Level detector

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1 Introduction

A pump is off when a specific input is low and stops when it is high. The aim is to start a pump by pushing a button and to stop it definitly when some water touches two copper electrodes.

2 Circuit description

2.1 Detector

The level detection is build around one Op Amp used as a follower, which non-inverting input is fed by the middle point of a resistance bridge. The upper resistance is the resistance R_w between the copper terminal. It is almost infinite when there is no water and about 1 Mo with water. The lower resistance R_b is 5.6 MΩ. The input voltage of the Op Amp is therefore

$$V_i = V_{cc}\frac{R_b}{R_b + R_w} \tag{1}$$

that is almost 0 V when there is no water, and, when there is water, it is about $5.6/(1 + 5.6) \times V_{cc}$, that is almost V_{cc} (which is 5V here).

This feeds the inverting input of a comparator, which non-inverting input is maintained at about $V_{cc}/2$ by a resistance bridge. Therefore, when the $-$ input is lower than $V_{cc}/2$ (no water), the output is high, and when it is higher than $V_{cc}/2$ (water), the output becomes low. The reaction resistance is used to introduce an hysteresis, so that if the $-$ input of the comparator undergoes some oscillations around $V_{cc}/2$, there is no spurious transition. The output resistance connected to V_{cc} is necessary to be chained with the logic 74AC circuits, because the output of the comparator is open-collector.

In summary **output of comparator is high when there is no water, and low when there is water.**

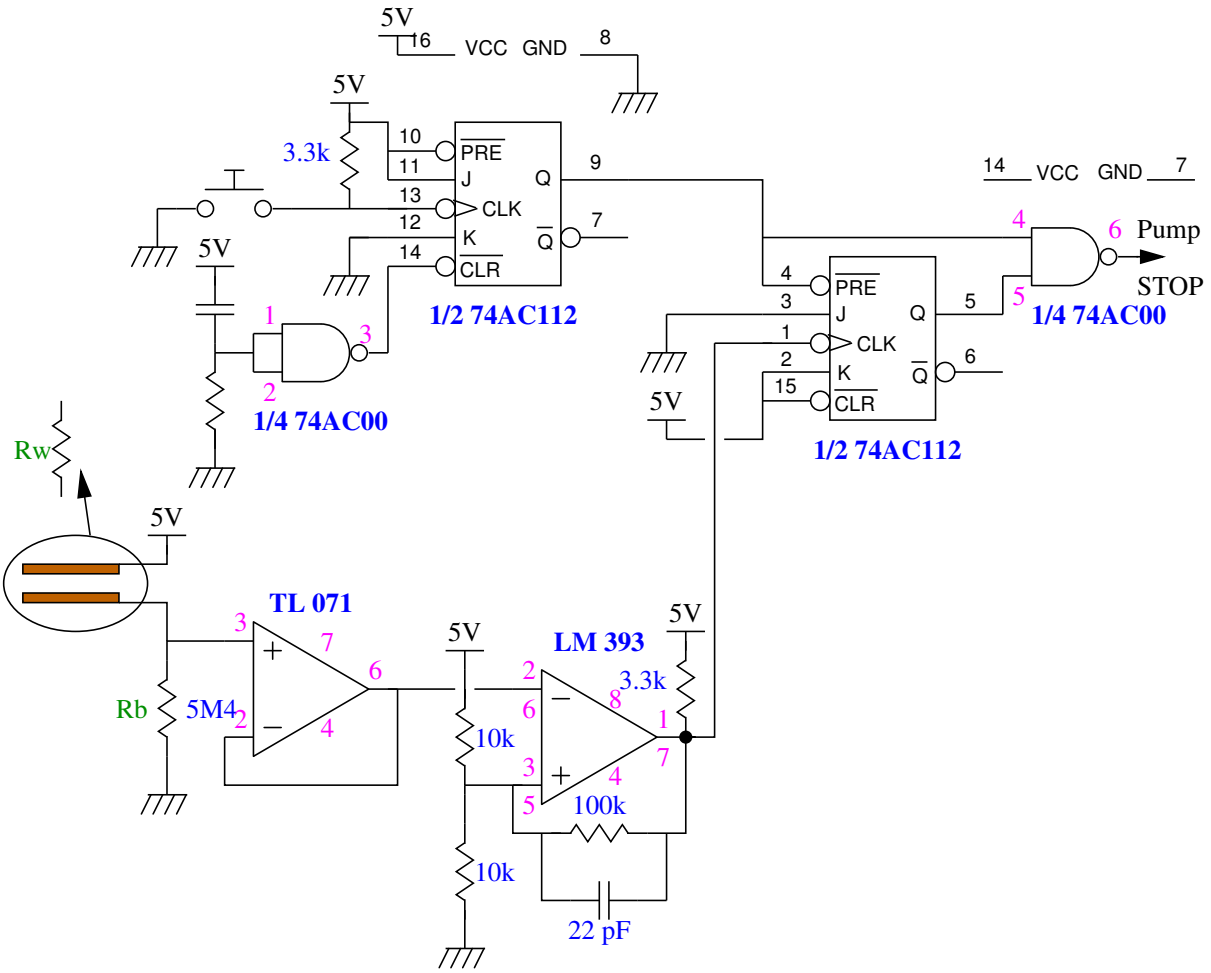

Figure 1: Circuit for the level detector

2.2 Logic circuit

The 74AC112 is a double JK flip-flop, switching on a high to low signal. Its logical table is presented in Fig. 2

2.2.1 Switching on the circuit

Let's look first at the left half JK (named JK1) and the NAND connected on its input CLR. Initially C is not charged so that the input of the NAND is 5V, the input CLR is low. This forces the output Q of JK1 to low. Two consequences:

- the output of the second NAND connected to the pump is high, the pump is stopped,
- the input PRE of the second JK is low which forces its output to high.

FUNCTION TABLE
(each flip-flop)

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

† Output states are unpredictable if $\overline{PRE}$ and $\overline{CLR}$ go high simultaneously after both being low at the same time.

Figure 2: Logical table of the 74AC112 JK flip-flops.

2.2.2 Circuit ready

Once the capacitor C is charged, the input of the NAND gate goes to ground. The input CLR of JK1 goes to high, so that the flip-flop is ready to use. Its output remains identical (see 4^{th} line of Fig. 2), so that nothing changes for JK2.

2.2.3 Starting the pump

If the button is pushed, input CLK of JK1 goes down, so that its output Q takes the state of input J, which is high. Two consequences:

- the input PRE of JK2 is now high, so that it is ready to go. Its output remains high, as far as no down signal comes on CLK.
- the other output of the right NAND is now also high, so that its output goes to low. The pump starts.

2.2.4 Stopping the pump

Finally, when the cell is full, the output of the comparator becomes low, which triggers JK2: thus, Q takes the state of its input J, and becomes low. This makes the output of the NAND to go high, which again stops the pump.

2.2.5 Summary

The next table summarizes the behaviour of the whole circuit

	$\overline{\text{PRE}}_1$	$\overline{\text{CLR}}_1$	J_1	K_1	Q_1	$\overline{\text{PRE}}_2$	$\overline{\text{CLR}}_2$	J_2	K_2	Q_2	$P = Q_1$ NAND Q_2
Switching on	H	L	H	L	L	L	H	L	H	H	H
Ready	H	H	H	L	L	L	H	L	H	H	H
Filling	H	H	H	L	H	H	H	L	H	H	L
Stopped	H	H	H	L	H	H	H	L	H	L	H